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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,365	11/12/2003	Johannes Becker	BECKER 1	6816

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EXAMINER	
DEBNATH, SUMAN	
ART UNIT	PAPER NUMBER
2435	

NOTIFICATION DATE	DELIVERY MODE
07/08/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)	
	10/706,365	BECKER, JOHANNES	
	Examiner	Art Unit	
	SUMAN DEBNATH	2435	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-11,13-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-11, 13-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 6-11, 13-18 and 20 are pending in this application.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office Action.

Claim Rejections - 35 USC § 103

3. Claims 1-4, 8-11 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mote, Jr. (Patent No.: US 5,631,912) (hereinafter, "Mote") further in view of Bos et al. (Patent No.: US 7,124,340 B1) (hereinafter, "Bos").

4. As to claim 1, Mote discloses for use with an integrated circuit (IC) having a testing port, a system for denying access to a memory in said IC (abstract) comprising:

port inhibit circuitry located on said IC and modifiable to achieve a configuration that determines an extent to which said testing port is enabled, said extent selected from the group consisting of: fully enabled, only partially disabled, and completely disabled (col. 4, lines 31-62, "[t]he output enable bit held in the latch 217 can be used to enable or disable the entire memory bus interface 148 when in JTAG test mode", see also, col. 4, lines 17-30 and col. 6, lines 10-34); and port access circuitry coupled to said testing port, that disables said testing port based on said configuration and denies access to said memory when said testing port is disabled (col. 4, lines 31-62, see also, col. 4, lines 17-30 and col. 6, lines 10-34).

Mote doesn't explicitly disclose wherein said testing port comprises a direct loopback between input and output pins thereof. However, Bos discloses wherein the testing port comprises a direct loopback between input and output pins thereof (column 7, lines 60-67 and column 8, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Mote as taught by Bos in order to isolate defects within the circuit by supporting loopback testing.

5. As to claims 8 and 15, these are rejected using the similar rationale as for the rejection of claim 1.

6. As to claim 2, the combination of Mote and Bos disclose wherein said testing port is a Joint Test Action Group (JTAG) port (Mote: col. 4, lines 31-62, see also, col. 4, lines 17-30 and col. 6, lines 10-34).

7. As to claims 9 and 16, these are rejected using the similar rationale as for the rejection of claim 2.

8. As to claim 3, the combination of Mote and Bos disclose wherein said port inhibit circuitry comprises an inhibit bit in a one-time programmable register (Mote: col. 4, lines 31-62, see also, col. 4, lines 17-30 and col. 6, lines 10-34).

9. As to claims 10 and 17, these are rejected using the similar rationale as for the rejection of claim 3.

10. As to claim 4, the combination of Mote and Bos disclose wherein said port inhibit circuitry is configured to be permanently modified prior to delivering said IC to a user thereof (Mote: col. 4, lines 31-62, see also, col. 4, lines 17-30 and col. 6, lines 10-34).

11. As to claim 6, the combination of Mote and Bos disclose wherein the testing port comprises a direct loopback between input and output pins thereof (Bos: column 7, lines 60-67 and column 8, lines 1-10).

12. As to claim 13, it is rejected using the similar rationale as for the rejection of claim 6.

13. As to claims 11 and 18, these are rejected using the similar rationale as for the rejection of claim 4.

14. Claims 7, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mote and further in view of Bos and Hansford (Patent No.: US 6,522,100 B2).

15. As to claim 7, neither Mote nor Bos explicitly disclose wherein said IC is a baseband chip of a mobile communication device. However, Hansford discloses

wherein the IC is a baseband chip of a mobile communication device (column 1, lines 45-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Mote and Bos as taught by Hansford in order to receive a frequency signal or frequency information.

16. As to claims 14 and 20, these are rejected using the similar rationale as for the rejection of claim 7.

17. Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may be applied as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Response to Arguments

18. Applicant's arguments filed April 06, 2010 have been fully considered but they are not persuasive.

19. Applicant argues that: "[t]he cited combination of Mote and Bos do not teach or suggest port access circuitry on a integrated circuit (IC) that denies access to a memory of the IC when a testing port is disabled as recited in pending independent Claims 1, 8, and 15."

Examiner maintains that Mote discloses port access circuitry on a integrated circuit (IC) that denies access to a memory of the IC when a testing port is disabled ("[t]he output enable bit held in the latch 217 can be used to enable or disable the entire memory bus interface 148 when in JTAG test mode" –e.g. see, col. 4, lines 31-62. see also FIG. 1; wherein IC 128 controls the access to memory system 140 through interface 148; access to memory 140 can either me disabled or enabled when in JTAG testing mode).

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUMAN DEBNATH whose telephone number is (571)270-1256. The examiner can normally be reached on 8 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y. Vu can be reached on 571 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. D./
Examiner, Art Unit 2435
/Kimyen Vu/
Supervisory Patent Examiner, Art Unit 2435